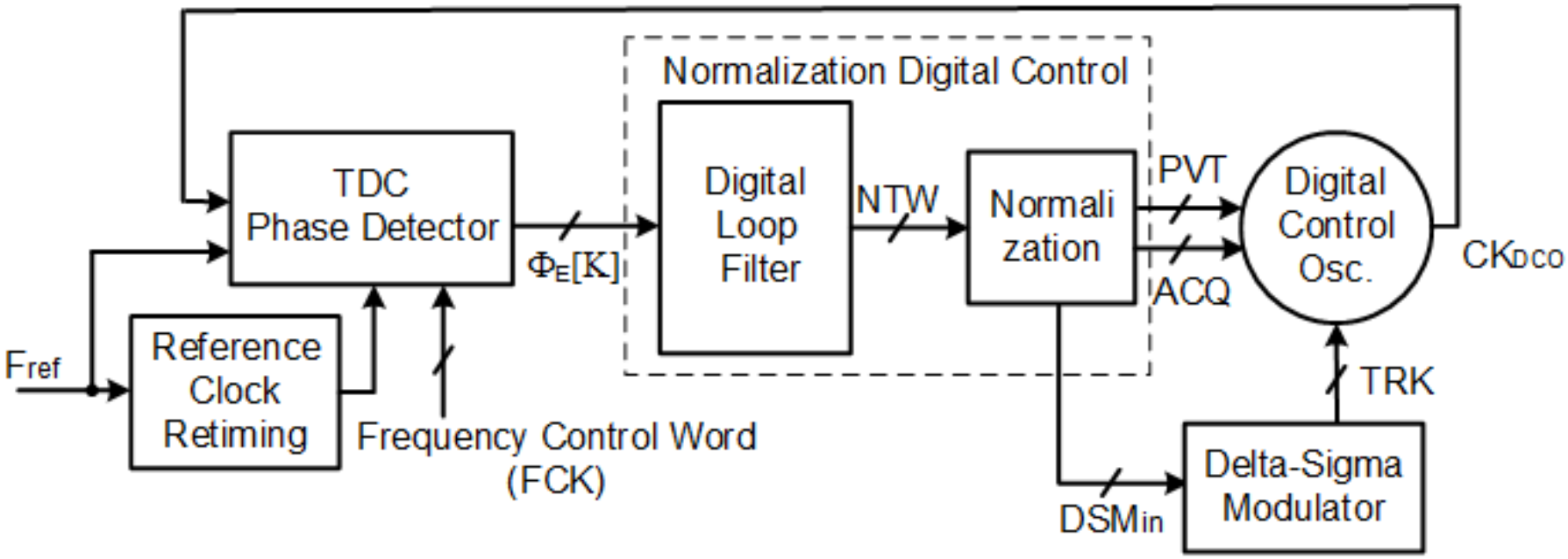
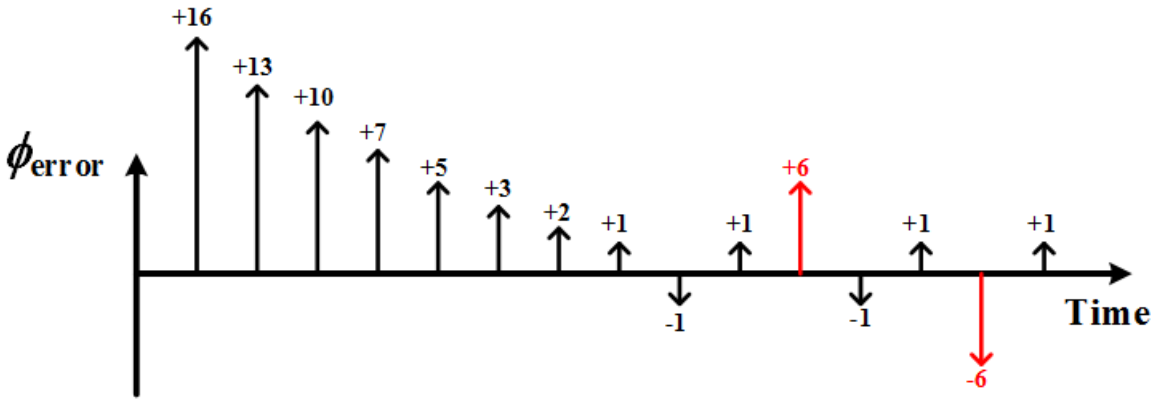
ADPLL Architecture

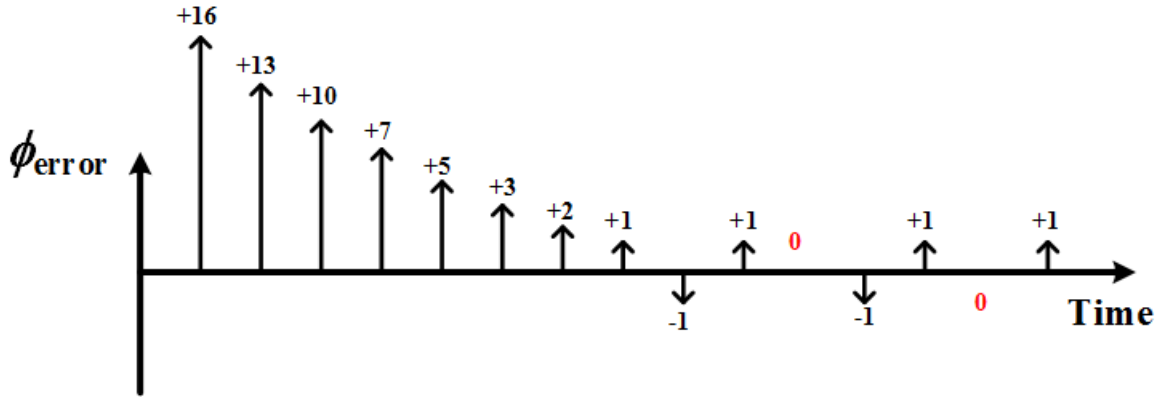


Median Filter

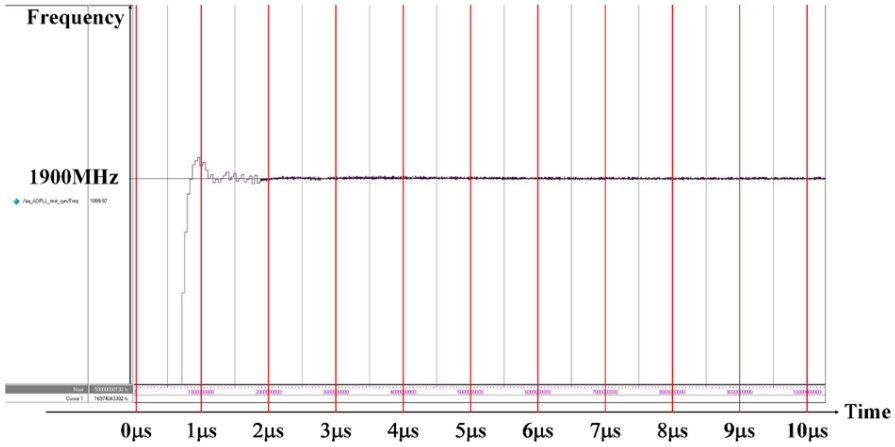
Original

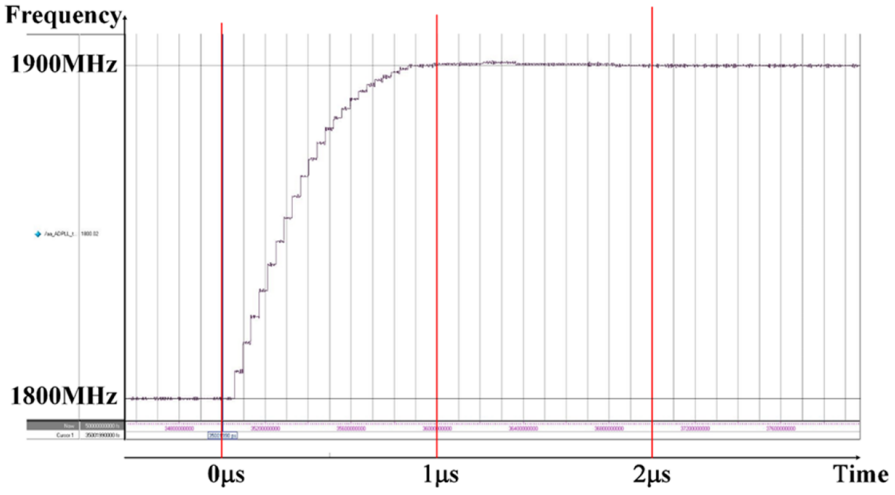


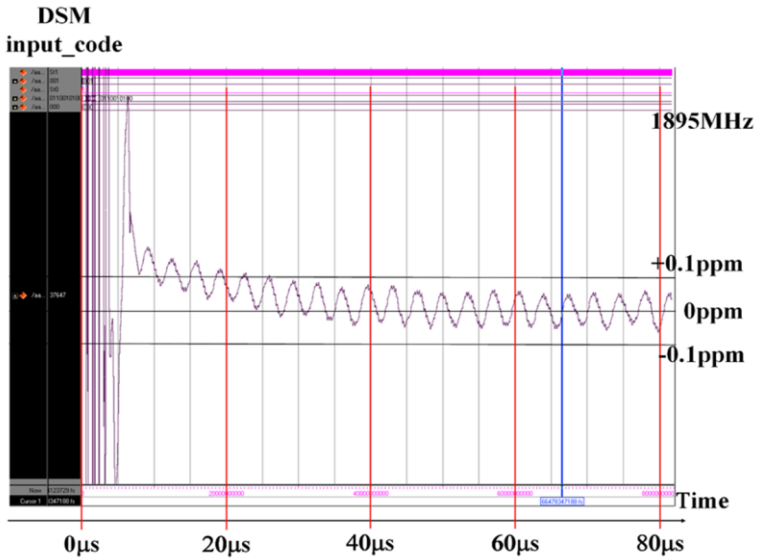
Median



Simulation Results







	Pre-simulation	Post-simulation
Reference frequency(MHz)	26	26
Frequency range(GHz)	1.785 - 2.103	1.759 - 2.081
Phase noise(dBc/Hz)	-121.3 @1MHz	-111.2 @1MHz
Resolution(Hz)	0.7	1.2
Locking time(μs)	< 1	< 2
Normalized locking time (cycle)	< 30	< 55
Supply voltage(V)	1.2	1.2
Power(mW)	9.72	11.24
Area(mm^2)	0.725× 0.973 = 0.71	

Comparison Table

	This Work [Post sim.]	[7] ISSCC'13	[8] JSSC'12	[9] JSSC'10	[10] JSSC'10	[2] JSSC'10	[11] JSSC'11
PFD/DCO Architecture	TDC / LC	TDC/LC	TDC / LC	TDC / LC	TDC / LC	TDC / LC	TDC / LC
Process(nm)	90	65	65	65	90	90	65
Reference frequency(MHz)	26	100	40	12.3	40	40	40
Frequency range (GHz)	3.6-4.2 (1.8-2.1)	57-64 (1.78-2.0)	2.9-4.0 (1.45-2.0)	2.29-2.92	2.1-2.8	9.75-10.17 (2.43-2.54)	2.9-4.0 (1.45-2.0)
Phase noise (dBc/Hz)	-111 @1MHz	-107.5 @1MHz	-110 @1MHz	-112 @1MHz	-115 @1MHz	-100 @1MHz	-139 @20MHz
Bandwidth(kHz)	N/A	N/A	312	40	500	N/A	312
Locking time(μs) (Nomalized cycle)	2.7 (71)	3 (300)	117 (4680)	30 (369)	<10 (behavioral) (400)	6.9 (276)	400 (16000)
Area(mm^2)	0.71	0.48	0.5	0.24	0.37	0.352	0.22
Power(mW)	11.24	48	5	12	9.72	7.1	4.5